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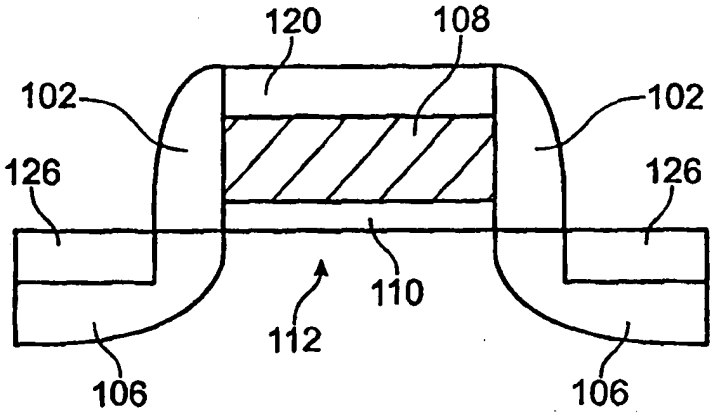
(54) Title: AMORPHIZATION OF SUBSTRATE TO PREVENT SILICIDE ENCROACHMENT INTO CHANNEL REGION OF FIELD EFFECT TRANSISTOR

(57) Abstract

A MOSFET includes silicided source/drain terminals and a substantially metal-free channel region, wherein the metal is characterized in that it diffuses more easily into the material of the substrate which contains the source/drain terminals than the material of the substrate diffuses into the metal. In a further aspect of the present invention, a portion of the source/drain terminals of a MOSFET are converted to an amorphous material prior to being reacted with a metal.



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AMORPHIZATION OF SUBSTRATE TO PREVENT SILICIDE ENCROACHMENT INTO CHANNEL REGION OF FIELD EFFECT TRANSISTOR

Background of the Invention

Field of the Invention

The invention relates to the field of semiconductor integrated circuits, and more particularly relates to metal-oxide-semiconductor field effect transistors.

Background

For many years integrated circuits incorporating metal-oxide-semiconductor field effect transistors (MOSFETs) have been manufactured with materials such as doped polycrystalline silicon to form the gate electrode, and doped crystalline silicon to form the source/drain terminals. Significant effort has been devoted to scaling down the physical dimensions of MOSFETs in order to increase the functionality of integrated circuits by including more transistors on each integrated circuit.

As devices were scaled down in size, there was a corresponding increase in the resistances associated with both the gate electrode and the source/drain terminals. Typically, as the linear dimensions of transistors were reduced, the thickness of the polycrystalline silicon that made up the gate electrode was also reduced. With both the width and thickness of the polycrystalline silicon reduced, the cross-sectional area of the gate electrode was reduced, which resulted in greater electrical resistance to signals propagating along the gate electrode. Similarly, the source/drain terminals became more resistive as their thickness, i.e., junction depths, were reduced, as required for maintaining appropriate electrical characteristics in the scaled down MOSFETs.

What is needed are structures that provide low sheet resistivities for MOSFET source/drain terminals and gate electrodes, and methods for making the same.

Summary of the Invention

Briefly, a MOSFET includes silicided source/drain terminals and a substantially metal-free channel region, wherein the metal is characterized in that it diffuses more easily into the material of the substrate which contains the source/drain terminals than the material of the substrate diffuses into the metal.

In a further aspect of the present invention, a portion of the source/drain terminals of a MOSFET are converted to an amorphous material prior to being reacted with a metal.

Brief Description of the Drawings

Fig. 1 is a schematic cross-sectional view of a FET having sidewall spacers and a layer of metal overlying the source/drain terminals, sidewall spacers, and gate electrode.

Fig. 2 is a schematic cross-sectional view of the FET of Fig. 1, after the layer of metal has been reacted with the source/drain terminals and the gate electrode.

Fig. 3 is a schematic cross-sectional view of the FET of Fig. 1, wherein the metal is highly diffusive in the substrate and after the layer of metal has been reacted with the source/drain terminals and the gate electrode, resulting in metal in the transistor channel region.

Fig. 4 is a schematic cross-sectional view of a FET showing a gate electrode overlying a gate dielectric layer formed on the surface of a substrate, sidewall spacers disposed adjacent the gate electrode, and source/drain terminals self-aligned to the gate electrode and sidewall spacers.

Fig. 5 is a schematic cross-sectional view of the FET of Fig. 4, after a portion of the source/drain terminals has been converted from a crystalline form to an amorphous form.

Fig. 6 is a schematic cross-sectional view of the structure of Fig. 5, after a layer of metal, which is highly diffusive in the substrate, has been formed over the source/drain terminals, sidewall spacers, and gate electrode.

Fig. 7 is a schematic cross-sectional view of the structure of Fig. 6, after the metal has been reacted with the amorphous portion of the source/drain terminals and the gate electrode.

Fig. 8 is a flow diagram illustrating process operations in accordance with the present invention.

Detailed Description

The terms, chip, integrated circuit, monolithic device, semiconductor device, and microelectronic device, are often used interchangeably in this field. The present invention is applicable to all the above as they are generally understood in the field.

The term "gate" is context sensitive and can be used in two ways when describing integrated circuits. Gate refers to a circuit for realizing an arbitrary logical function when used in the context of a logic gate. However, as used herein, gate refers to the insulated gate terminal of a three terminal FET when used in the context of transistor circuit configurations or formation of transistor structures. The expression "gate terminal" is generally interchangeable with the expression "gate electrode". A FET can be viewed as a four terminal device when the semiconductor body is considered. However, for the purpose of describing illustrative embodiments of the present invention, the FET will be described using the traditional gate-drain-source, three terminal model.

Channel, as used herein, refers to that portion of the semiconductor body that underlies the gate dielectric, is bounded by the source/drain terminals, and is the region of the FET where current flows between the source and drain terminals.

Polycrystalline silicon is a nonporous form of silicon made up of randomly oriented crystallites or domains. Polycrystalline silicon is often formed by chemical vapor deposition from a silicon source gas or other methods and has a structure that contains large-angle grain boundaries, twin boundaries, or both. Polycrystalline silicon is often referred to in this field as polysilicon, or sometimes more simply as poly.

Silicide refers generally to Si-metal compounds.

Salicide refers generally to silicide that is self-aligned to some structure, for example, a silicide self-aligned to a FET gate structure.

Source/drain terminals refer to the terminals of a FET, between which conduction occurs under the influence of an electric field, subsequent to the inversion of the semiconductor surface under the influence of another electric field resulting from a voltage applied to the gate terminal. Generally, the source and drain terminals are fabricated such that they are geometrically symmetrical. With geometrically symmetrical source and drain terminals it is common to simply refer to these terminals as source/drain terminals, and this nomenclature is used herein. Designers often designate a particular source/drain terminal to be a "source" or a "drain" on the basis of the voltage to be applied to that terminal when the

FET is operated in a circuit. Typically, source/drain terminals are doped with either donor (n-type) or acceptor (p-type) atoms to create the desired electrical characteristics.

As FETs have been scaled down in dimension, a common approach to decreasing the resistivities associated with the scaled down source/drain terminals and gate electrodes, has been to form a layer having a relatively low sheet resistivity, in parallel with the source/drain terminals, and also to form such a layer in parallel with the gate electrodes. For example, various refractory metal silicides (e.g., titanium silicide) were formed over the surfaces of the source/drain terminals and gate electrodes, respectively. In this way, the effective sheet resistivity of both the source/drain terminals and gate electrodes was reduced.

An advantage of such a process, in addition to lowering the sheet resistivities mentioned above, is that the source/drain terminals and gate electrodes can be salicided in the same (i.e., a concurrent) process operation. This is true because the metals typically chosen to form the salicided regions react with both the doped crystalline silicon of the source/drain terminals and the polycrystalline silicon of the gate electrodes.

Referring to Figs. 1 and 2, a prior art process and structure, which includes silicided source/drain terminals and gate electrode, are described. More particularly, Fig. 1 is a schematic cross-sectional view showing a prior art FET **100** having sidewall spacers **102** and a layer of metal **104** overlying a pair of source/drain terminals **106**, sidewall spacers **102**, and a gate electrode **108**. Gate electrode **108** overlies a gate dielectric layer **110**. Also, as can be seen in Fig. 1, a channel region **112** exists between source/drain terminals **106** and below gate dielectric **110**. In typical prior art implementation examples, such as the one shown here, metal layer **104** is titanium.

Fig. 2 shows a schematic cross-sectional view of FET **100** of Fig. 1, after metal layer **104** has been reacted with source/drain terminals **106** and gate electrode **108**. In such an implementation, the titanium of metal layer **104** reacts with the crystalline silicon of source/drain terminals **106** and the polysilicon of gate electrode **108** to form titanium silicide layers as indicated in Fig. 2.

Unfortunately, as described above, continued aggressive scaling of FET dimension into the deep submicron region has created a need to reduce sheet resistivities to a greater extent than appears to be possible using conventional titanium silicide processing. Fig. 3 shows a schematic cross-sectional view of FET **100** of Fig. 1, wherein an alternative metal layer **104** comprises a metal that is highly diffusive in the substrate and after metal layer **104** has been reacted with source/drain terminals **106** and gate electrode **108**. In this case, the metal reacts with gate electrode **108** to form low resistance layer **120**, and reacts with source/drain terminals **106** to form low resistance layers **118**. As shown in Fig. 3, low resistance layer **118** extends laterally through source/drain terminal **106** resulting in metal atoms physically occupying locations in transistor channel region **112**. This phenomenon may also be referred to as silicide encroachment into the transistor channel. In this case, a metal such as nickel has been used, rather than titanium as shown in the example of Fig. 2. Although lower sheet resistivities can be obtained through the use of nickel rather than titanium, such implementations have been observed to suffer from yield limiting transistor malfunctions. These malfunctions result from the movement of metal atoms, nickel in this case, into the substrate material, silicon in this case. Those skilled in the art and having the benefit of this disclosure will recognize that silicide encroachment may occur not just into the channel region but also into the semiconductor body terminal of the FET.

Embodiments of the present invention include salicided source/drain terminals wherein the metal salicide is formed from a metal that is highly diffusive in a substrate material such as, but not limited to, silicon. An illustrative embodiment of the present invention is described in conjunction with Figs. 4-7.

Fig. 4 shows a schematic cross-sectional view of a FET having gate electrode **108** overlying gate dielectric layer **110** formed on the surface of a substrate. Sidewall spacers **102** are disposed adjacent gate electrode **108**, and source/drain terminals **106** are self-aligned to gate electrode **108** and sidewall spacers **102**. That is, source/drain terminals **106** are substantially adjacent to sidewall spacers **102** and gate electrode **108**. Additionally, although source/drain terminals **106** are shown completely disposed in the substrate in Fig. 4, it will be recognized that source/drain terminals may be partially in the substrate and partially raised above the substrate. No limitation on the exact geometries of the various constituent parts of

the FET are intended herein. The transistor structure shown in Fig. 4 is known in the art and is formed by well known and commonly understood microelectronic process operations such as photolithography, etching, oxidation, thin film deposition, and so on. A transistor such as that shown in Fig. 4 may then be further processed, in accordance with the present invention, in order that salicided source/drain terminals may be formed with metals that are highly diffusive in silicon.

Fig. 5 shows a schematic cross-sectional view of the FET of Fig. 4, after a portion of source/drain terminals **106** has been converted from a crystalline form to an amorphous form. That is an amorphous silicon (a-Si) layer **122** is created in an upper region of source/drain terminals **106**. In this case, upper region refers to those portions of source/drain terminals **106** that are relatively closer to the surface of the substrate than other portions of source/drain terminals **106**. In the illustrative embodiments of the present invention, a-Si layers **122** are formed by the ion implantation of silicon into the surface of source/drain terminals **106**.

Implant species, dose, and energy are selected to achieve a specific amorphous depth. The targeted depth of a-Si **122** is determined, at least in part, by the thickness of a metal layer with which a-Si **122** is to be reacted. By way of illustration and not limitation, if 20 nm of Ni are used, then an a-Si **122** depth of approximately 40 nm is selected. This can be accomplished by performing an ion implant operation of Si at an energy of approximately 20 keV and a dose of approximately $5x10^{14}/cm^2$. Alternatively, Ge ions may be implanted at, for example, an energy of 40kev and a dose of $2x10^{14}/cm^2$. Those skilled in the art and having the benefit of this disclosure will recognize that any suitable set of ion implantation specifications that produces an amorphous portion in the source/drain terminals may be used. The depth of the amorphous portion of the source/drain terminals is chosen such that the reaction between the metal and the amorphous silicon effectively results in the silicide remaining in the region of the source/drain terminals that was converted to amorphous form.

Fig. 5 also shows an amorphous region **123** that is formed in the upper portion of gate electrode **108**. Amorphous region **123** is created by the ion implantation that creates a-Si layers **122**.

Fig. 6 shows a schematic cross-sectional view of the structure of Fig. 5, after a layer of metal **124**, which is highly diffusive in the substrate, has been formed over a-Si **122** of source/drain terminals **106**, sidewall spacers **102**, and gate electrode **108**. In the illustrative embodiment, metal **124** is nickel. Metal **124** may be deposited by any suitable, well-known process such as, but not limited to, sputtering. Alternatively, metal **124** may be deposited by a physical vapor deposition (PVD) operation.

Fig. 7 shows a schematic cross-sectional view of the structure of Fig. 6, after metal **124** has been reacted with amorphous portion **122** of source/drain terminals **106** to form salicided regions **126**; and with gate electrode **108** to form salicided region **120**. In one embodiment of the present invention, the reaction conditions include placing the wafer into an N_2 ambient at approximately 500°C for approximately 10 seconds. Those skilled in the art will recognize that various ranges of times and temperatures may be used to achieve the desired reaction.

Referring to Fig. 8, a process **200** embodying the present invention is described. More particularly, an insulated gate FET structure, including gate electrode, gate insulator, and source/drain terminals, is formed **202** on a substrate in accordance with well-known microelectronic manufacturing operations. Subsequently, a portion of the source/drain terminals are converted **204** to amorphous form. When the substrate is a silicon wafer, the conversion operation is typically achieved by ion implantation of silicon. The implantation of silicon into the doped crystalline silicon regions that make up the source/drain terminals results in a layer of a-Si. A metal is deposited **206**, typically over the entire surface of the substrate. Those skilled in the art and having the benefit of this disclosure will recognize that a blanket deposition of metal, although typical, is not required by the present invention. The metal that is over the a-Si is reacted **208** with the a-Si, such that the a-Si is substantially consumed and a low resistance layer is formed. Typical reaction conditions include placing the wafer in an N_2 ambient at approximately 500°C, for approximately 10 seconds.

Conclusion

Embodiments of the present invention provide an a-Si/c-Si boundary to block silicide encroachment into the transistor channel. An a-Si region is typically produced in the

source/drain terminals by ion implantation prior to metal deposition. The a-Si depth is chosen such that it will just be consumed by the metal to form silicide, and such that substantially none of the a-Si remains after the silicidation process. The metal is believed to react preferentially with the a-Si to form the silicide because the a-Si has a higher energy than c-Si and is therefore more reactive. As a result, the boundary between the a-Si and c-Si essentially serves as a barrier against further reaction or metal diffusion into the c-Si substrate.

An advantage of embodiments of the present invention is lower sheet resistivities for polysilicon and source/drain terminals than is achievable with other metal silicides such as titanium silicide.

A further advantage of the present invention is that encroachment of metal into the channel region of field effect transistors is avoided.

It will be understood by those skilled in the art that many design choices are possible within the scope of the present invention. For example, metals such as, but not limited to cobalt (Co) may be used rather than nickel. Additionally, the present invention is not limited to silicon substrates.

It will be understood that various other changes in the details, materials, and arrangements of the parts and steps which have been described and illustrated may be made by those skilled in the art without departing from the principles and scope of the invention as expressed in the subjoined Claims.

What is claimed is:

1. A method of forming a transistor, comprising:

forming a gate electrode superjacent a substrate;

forming sidewall spacers adjacent to the gate electrode;

forming source/drain terminals substantially adjacent to the sidewall spacers;

converting a portion of the source/drain terminals to an amorphous form;

depositing a metal over the gate electrode, and source/drain terminals; and

reacting the metal with the amorphous portion of the source/drain terminals.

2. The method of Claim 1, further comprising forming a gate dielectric layer disposed between the substrate and the gate electrode.

3. The method of Claim 1, wherein converting a portion of the source/drain terminals to an amorphous form comprises bombarding the source/drain terminals with particles.

4. The method of Claim 3, wherein the particles comprise ions.

5. The method of Claim 1, wherein converting a portion of the source/drain terminals to an amorphous form comprises implanting Si at an energy of approximately 20keV and a dose of approximately $5x10^{14}/cm^2$.

6. The method of Claim 1, wherein the substrate comprises crystalline silicon; and converting a portion of the source/drain terminals to an amorphous form comprises ion implanting portions of the substrate.

7. The method of Claim 6, wherein ion implanting comprises implanting Ge at an energy of approximately 40 keV and a dose of approximately $2x10^{14}ions/cm^2$.

8. The method of Claim 1, wherein the metal is selected from the group consisting of nickel and cobalt.

9. The method of Claim 1, wherein reacting comprises placing the substrate in an N_2 ambient at approximately 500°C, for approximately 10 seconds.

10. A method of forming a field effect transistor comprising:

forming a gate insulator layer over a substantially crystalline silicon substrate;

forming a polysilicon layer over the gate insulator layer;

patterning the polysilicon and gate insulator layers to form at least one gate electrode;

forming sidewall spacers adjacent to the at least one gate electrode;

forming source/drain terminals in the substrate substantially adjacent to the sidewall spacers;

forming an amorphous portion in the source/drain terminals;

depositing a metal over the at least one gate electrode, and source/drain terminals; and

reacting the metal with the amorphous portion of the source/drain terminals.

11. The method of Claim 10, wherein forming an amorphous portion in the source/drain terminals comprises ion implanting the source/drain terminals.

12. The method of Claim 10 wherein the metal is nickel.

13. The method of Claim 10 wherein the metal is cobalt.

14. The method of Claim 10 wherein the metal diffuses more easily into a material of the substrate than the material of the substrate diffuses into the metal.

15. A method of forming a silicided region in a substrate, comprising:

forming an amorphous region in the substrate;

depositing a metal layer over the amorphous region; and

reacting the metal with the amorphous region.

16. The method of Claim 15, wherein the substrate comprises crystalline silicon; and forming an amorphous region in the substrate comprises implanting ions into at least a portion of the substrate.

17. The method of Claim 16, wherein implanting comprises implanting silicon.

18. The method of Claim 16, wherein implanting comprises implanting germanium.

19. A field effect transistor; comprising:

a gate insulator disposed on a substrate, the substrate comprising a first material;

a gate electrode disposed over the gate insulator;

at least one source/drain terminal substantially disposed in the substrate, substantially adjacent the gate electrode; and

a silicide disposed in the source/drain terminal;

wherein the silicide comprises a metal that diffuses more easily into the first material than the first material diffuses into the metal.

20. The field effect transistor of Claim 20, wherein the first material comprises silicon; and the metal is selected from the group consisting of nickel and cobalt.

Fig. 1
(PRIOR ART)

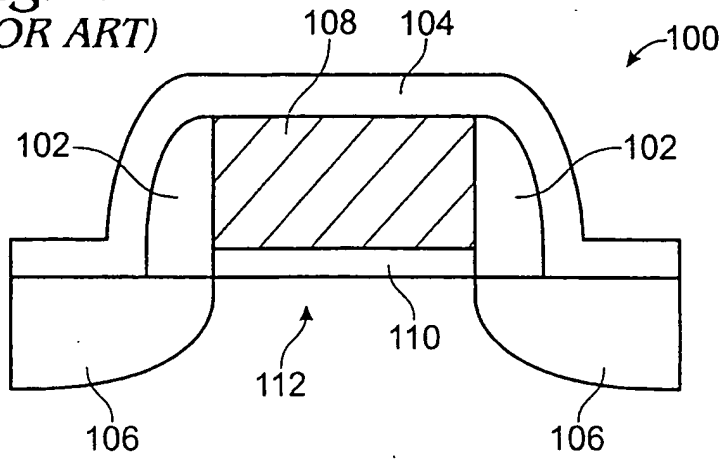


Fig. 2
(PRIOR ART)

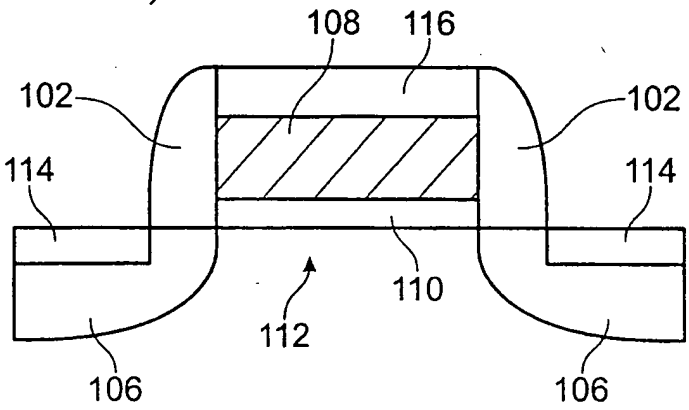


Fig. 3

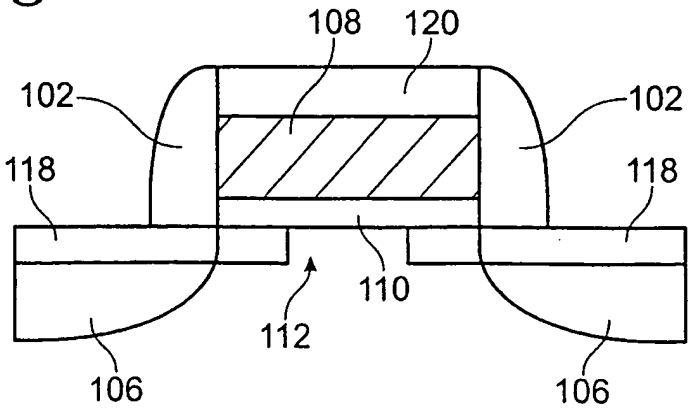


Fig. 4

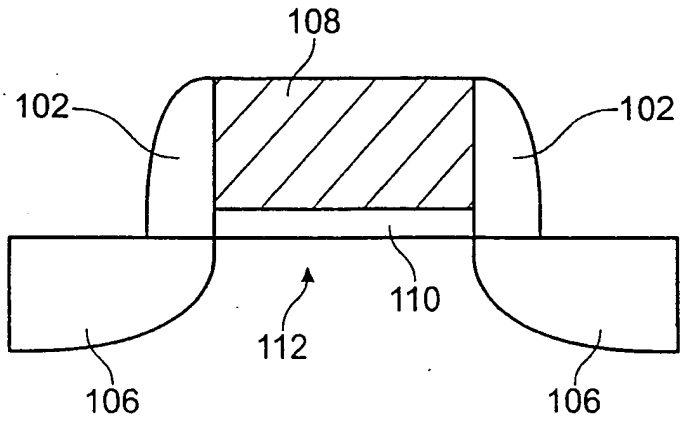


Fig. 5

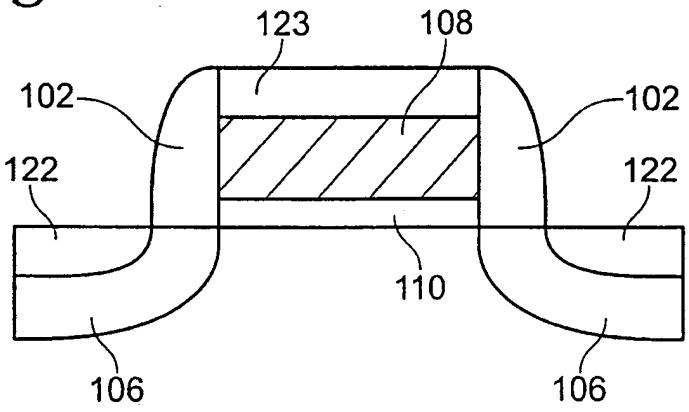


Fig. 6

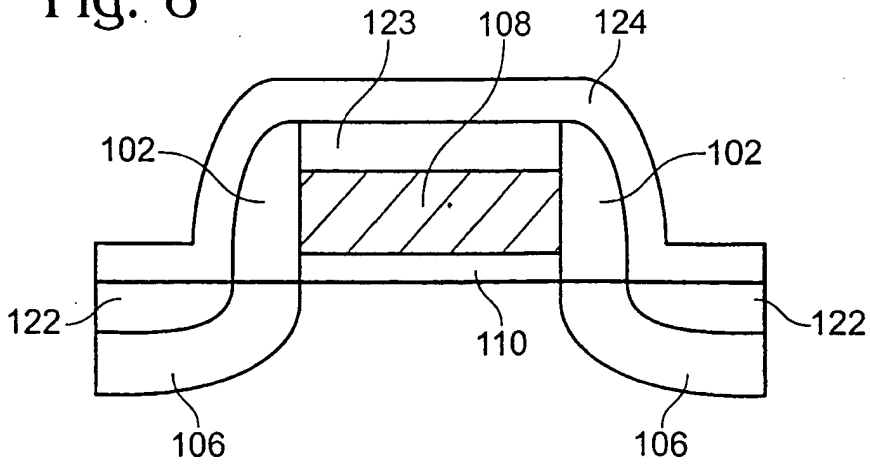
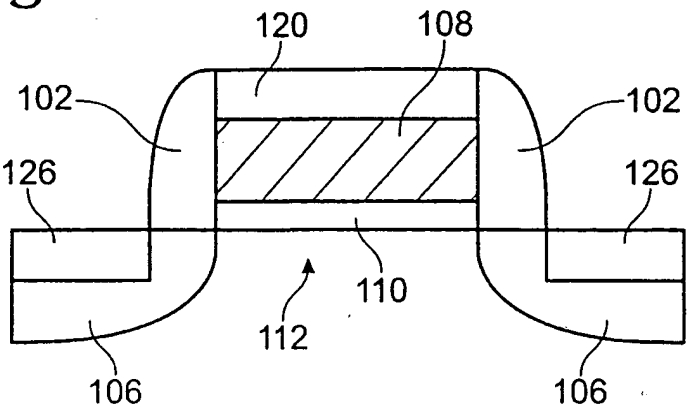


Fig. 7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102
126
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112
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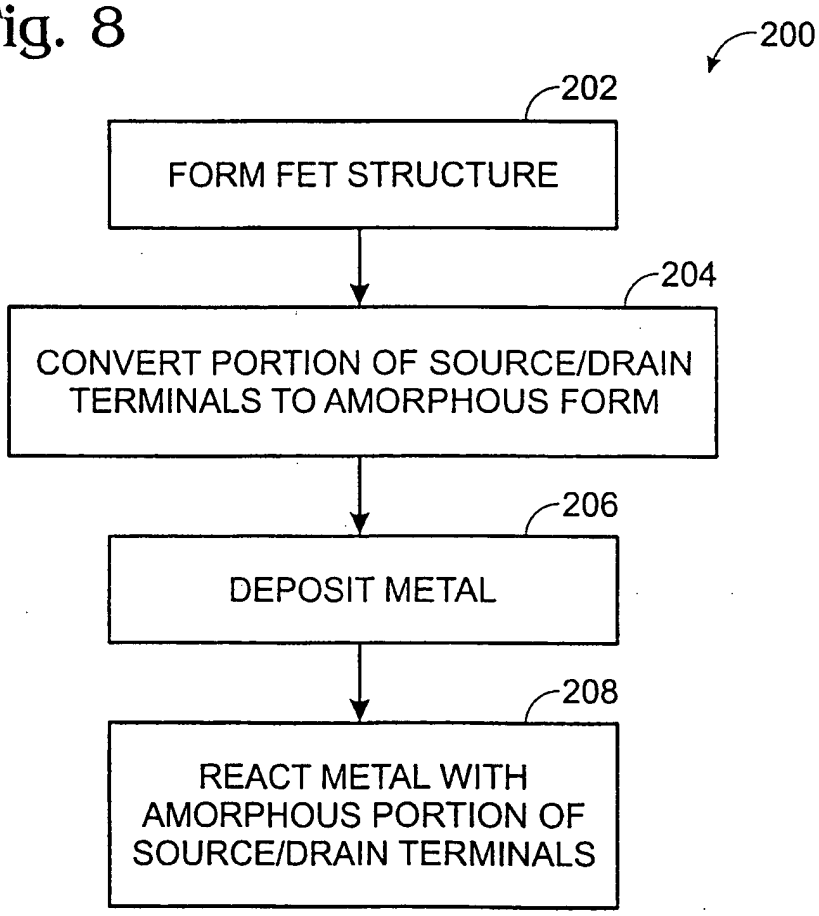
106

Fig. 8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206
DEPOSIT METAL
208
REACT METAL WITH AMORPHOUS PORTION OF SOURCE/DRAIN TERMINALS

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(81) Designated States *(national)*: AE, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, CA, CH, CN, CR, CU, CZ, DE, DK, DM, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TR, TT, TZ, UA, UG, US, UZ, VN, YU, ZA, ZW.

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Published:
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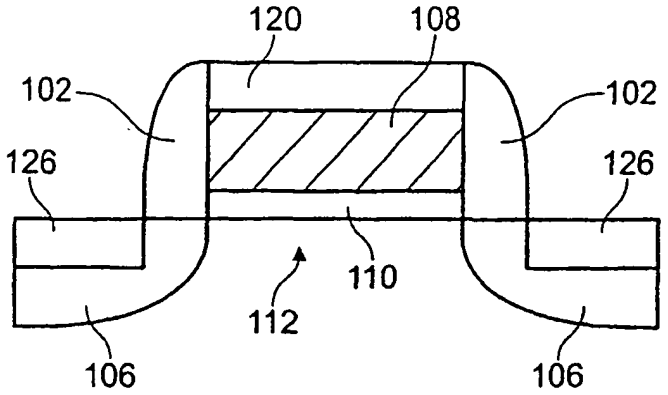
(88) Date of publication of the international search report:
27 June 2002

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

(54) Title: AMORPHIZATION OF SUBSTRATE TO PREVENT SILICIDE ENCROACHMENT INTO CHANNEL REGION OF FIELD EFFECT TRANSISTOR



(57) Abstract: A MOSFET includes silicided source/drain terminals (106) and a substantially metal-free channel region (112), wherein the metal is characterized in that it diffuses more easily into the material of the substrate which contains the source/drain terminals (106) than the material of the substrate diffuses into the metal. In a further aspect of the present invention, a portion of the source/drain terminals (106) of a MOSFET are converted to an amorphous material (122) prior to being reacted with a metal.

WO 00/36634 A3

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US99/26865

A. CLASSIFICATION OF SUBJECT MATTER

IPC(6) : H01L 29/76
US CL : 257/385, 386, 387, 388

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 257/385, 386, 387, 388

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 5,807,770 A (MINEJI) 15 September 1998 (15.09.98), col. 5, lines 6-28.	1-6, 10, 11, 15-19
X	US 5,766,997 A (TAKEUCHI) 16 June 1998 (16.06.98), col. 6, lines 44-68.	1-17, 19, 20
X	US 5,899,720 A (MIKAGI) 04 May 1999 (04.05.99), col. 5, lines 2-22.	1-11, 13, 19, 20
X	US 5,691,212 A (TSAI et.al.) 25 November 1997 (25.11.99),col 5,lines 14-67.	1-11, 13, 15, 18-20
X	US 5,710,450 A (CHAU et.al.) 20 January 1998 (20.01.98), col. 3, lines 4-65.	1-6
X	US 6,010,936 A (SON) 04 January 2000 (04.01.00), col 3, lines 3-58.	1-6, 8

[X] Further documents are listed in the continuation of Box C. [ ] See patent family annex.

*	Special categories of cited documents:	"T"	later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"A"	document defining the general state of the art which is not considered to be of particular relevance	"X"	document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"E"	earlier document published on or after the international filing date	"Y"	document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"L"	document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)	"&"	document member of the same patent family
"O"	document referring to an oral disclosure, use, exhibition or other means		
"P"	document published prior to the international filing date but later than the priority date claimed		

Date of the actual completion of the international search	Date of mailing of the international search report
02 FEBRUARY 2000	18 JUL 2000
Name and mailing address of the ISA/US Commissioner of Patents and Trademarks Box PCT Washington, D.C. 20231 Facsimile No. (703) 305-3230	Authorized officer EDGARDO ORTIZ Telephone No. (703) 308 - 0956

Form PCT/ISA/210 (second sheet)(July 1992)*

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US99/26865

C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	JP 405136398 A (HAYASHIDA) 06 June 1993 (06.06.93), abstract	1-6
Y	JP 362122173 A (IMAOKA) 03 June 1987 (03.06.87), abstract	1-6

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US99/26865

Box I Observations where certain claims were found unsearchable (Continuation of item 1 of first sheet)

This international report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:

2. ☐ Claims Nos.:
because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:

3. ☐ Claims Nos.:
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box II Observations where unity of invention is lacking (Continuation of item 2 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:

Please See Extra Sheet.

1. ☒ As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims.

2. ☐ As all searchable claims could be searched without effort justifying an additional fee, this Authority did not invite payment of any additional fee.

3. ☐ As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims for which fees were paid, specifically claims Nos.:

4. ☐ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:

Remark on Protest

☐ The additional search fees were accompanied by the applicant's protest.

☒ No protest accompanied the payment of additional search fees.

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US99/26865

BOX II. OBSERVATIONS WHERE UNITY OF INVENTION WAS LACKING
This ISA found multiple inventions as follows:

This application contains the following inventions or groups of inventions which are not so linked as to form a single inventive concept under PCT Rule 13.1. In order for all inventions to be searched, the appropriate additional search fees must be paid.

Group I, claim(s)1-18, drawn to a method of forming a transistor.
Group II, claim(s)19-20 , drawn to a field effect semiconductor device.

The inventions listed as Groups I and II do not relate to a single inventive concept under PCT Rule 13.1 because, under PCT Rule 13.2, they lack the same or corresponding special technical features for the following reasons: The claims relating to a method of forming a transistor contain the special technical feature consisting of an amorphousportion on the source/drain regions, whereas the claims relating to the field effect semiconductor device do not include the special technical feature described .